PVP 23

Code: 23ES1401

II B.Tech - II Semester – Regular / Supplementary Examinations
APRIL 2026

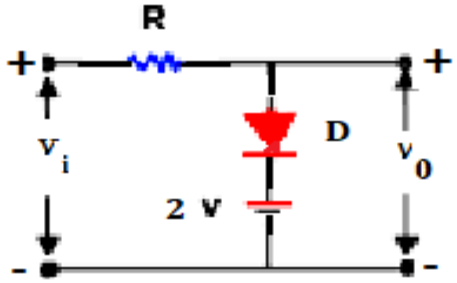
ANALOG CIRCUITS
(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level CO – Course Outcome

PART – A

		BL	CO1
1.a)	Draw the two circuits of clamping.	L1	CO1
1.b)	Draw the output waveform of the given clipper circuit with a sinusoidal input signal of 10Vp-p. Assume diode is ideal. V=2V, R=1kΩ 	L2	CO1
1.c)	Draw the exact h-parameter model of BJT in CE configuration.	L1	CO1
1.d)	Explain the effect of emitter bypass capacitor on frequency response of a CE amplifier.	L2	CO2
1.e)	Sketch the equivalent circuit of a Crystal.	L2	CO1
1.f)	Draw the circuit diagram of Op-amp inverting adder and write the expression for its output voltage.	L3	CO1

1.g)	For the given uA741 OP-AMP, operating in voltage Follower configuration, having $2V_{P-P}$ sinusoidal input, find the maximum frequency up to which it produces undistorted output.	L3	CO3
1.h)	Why level translator circuit is required in OP-AMP block diagram. Explain.	L2	CO2
1.i)	List the applications of 555 timer.	L1	CO5
1.j)	An7 bit D/A converter has a resolution of 20mv. Find the full scale voltage and output voltage when the input is 1101110.	L2	CO4

PART – B

			BL	CO	Max. Marks
UNIT-I					
2	a)	With the help of a neat circuit diagram, explain the working of a two level diode clipper and draw the output waveform.	L3	CO3	5 M
	b)	Derive the expression for Stability factor of Self bias circuit.	L3	CO4	5 M
OR					
3	a)	In a CE germanium transistor amplifier circuit, the bias is provided by self-bias. The various parameters are V_{cc}=16v, R_c=3kΩ, R_1=10kΩ, R_2=90kΩ, R_E=2kΩ, α=0.975. Determine i)coordinates of Q-point ii) stability factor.	L4	CO4	5 M
	b)	What is negative clamping and explain its working principle with input and output waveforms.	L3	CO3	5 M

UNIT-II					
4	a)	Derive the simplified CE h-parameter model from its exact h-parameter model.	L4	CO4	5 M
	b)	A CE amplifier has h-parameters given by h_{ie}=2000Ω, h_{re}=2x10^{-4},h_{fe}=80,h_{oe}=25x10^{-6} mho. If both load and source resistances are 1kΩ. Determine i)Current gain A_I ii)Voltage gain A_v	L4	CO4	5 M
OR					
5	a)	Analyze BJT CE amplifier using exact h-parameter model to derive its voltage gain, current gain and input impedance.	L4	CO4	6 M
	b)	Explain the low frequency response of a CE amplifier describing the effect of bypass capacitor, coupling capacitor and internal capacitors.	L3	CO3	4 M
UNIT-III					
6	a)	Derive the expression for frequency of oscillation of RC-phase shift oscillator.	L4	CO4	6 M
	b)	Explain the Ideal characteristics of an Op-Amp in detail.	L2	CO2	4 M
OR					
7	a)	Define and discuss about the AC characteristics of Op-Amp.	L4	CO4	3 M
	b)	What is a Crystal Oscillator? Explain its operation and advantages.	L3	CO3	7 M

UNIT-IV					
8	a)	Draw the Op-Amp Subtractor circuit and derive the expression for its output voltage.	L4	CO4	4 M
	b)	Discuss the operation of basic integrator using Op-Amp with neat sketches.	L3	CO3	6 M
OR					
9	a)	Describe the working of an Op-Amp square wave generator with the help of neat circuit diagram and waveforms.	L3	CO3	5 M
	b)	Explain the working of an Instrumentation Amplifier using three Op-Amps with a neat circuit diagram.	L3	CO3	5 M
UNIT-V					
10	a)	Explain the following specifications of Data converters: Resolution, Monotonicity, Settling time and Conversion time.	L2	CO2	4 M
	b)	Describe the operation of 555 timer with the help of its functional block diagram.	L3	CO5	6 M
OR					
11	a)	Discuss the function of a Voltage Controlled Oscillator and explain its applications.	L3	CO4	4 M
	b)	Explain the operation of Successive approximation type A/D converter with neat block diagram.	L3	CO5	6 M

II B.Tech II Sem – Regular / Supply Exam, April 2026

Analog Circuits (23ES1401)

Scheme of Valuation

part-A

1 a) positive clamper – 1M

Negative clamper – 1M

b) Output waveform – 2M

c) Exact CE hybrid model Circuit diagram – 2M

d) Effect of bypass capacitor – 2M

e) Equivalent circuit of a crystal – 2M

f) Inverting Adder/summer circuit diagram – 2M

g) formula – 1M

Calculation of 'f' – 1M

h) purpose of level translator circuit – 2M

i) any two applications of 555 Timer – 2M

j) V_{FS} – 1M

V_0 – 1M

part-B

2. a) Circuit Diagram – 2M

Diode ON, OFF conditions – 1M + 1M

Output waveform – 1M

b) Circuit diagrams of self bias – 3M

derivation of 'S' – 2M

3 a) i) Calculation of β, V_T, R_T – 2M

Q-point – 1M

ii) Stability factor – 2M

b) Circuit Diagram — 2M
operation — 1M
Waveforms — 2M

4 a) Exact CE hybrid model — 2M , Conditions — 1M
Approximate CE hybrid model — 2M

b) (i) Current gain — 2M , Voltage gain — 3M

5 a) Circuit Diagram — 2M , derivation of A_I, Z_i, A_V — 4M

b) Circuit Diagram and waveform — 2M
Effect of C_C, C_E, C_π, C_μ — 2M

6 a) main circuit, AC equivalent circuits — 3M
Derivation of f_o, conditions — 3M

b) Any three Ideal characteristics — 4M

7 a) Slew rate concept, formula — 3M

b) crystal oscillator, piezo electric effect — 1M
working, symbol, equivalent circuit — 2M
frequency response graph and operation with formulas — 4M

8 a) circuit diagram — 2M , derivation of V_o — 2M

b) circuit diagram with V_o expression — 4M , frequency response graph — 2M

9 a) Circuit diagram — 2M , operation — 1M , waveform — 2M

b) Circuit diagram — 2M , operation — 1M , V_o derivation — 2M

10 a) Resolution — 1M , monotonicity — 1M , Settling time — 1M , Conversion time — 1M

b) Block diagram — 3M , operation — 3M

11 a) function of VCO — 1M , any three applications — 3M

b) Block diagram — 4M
operation — 2M

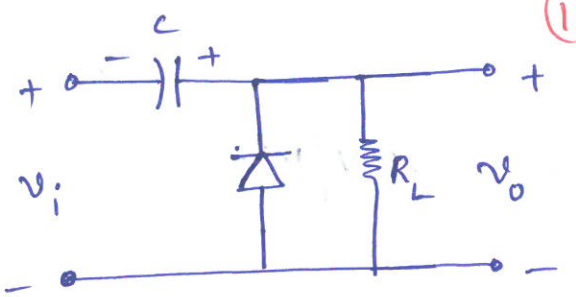
II B.Tech II-Sem Regular Exams, April 2026.

Subject - Analog Circuits

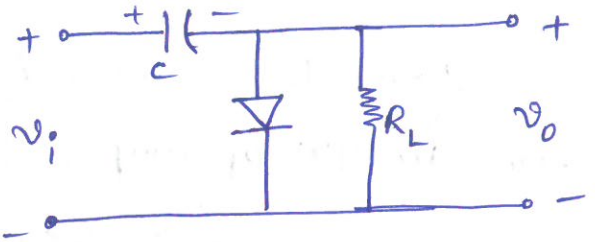
Key

Part-A

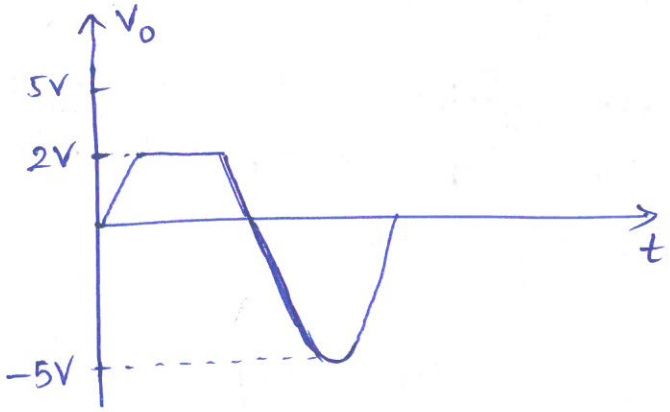
1. a) positive clamper (1M)



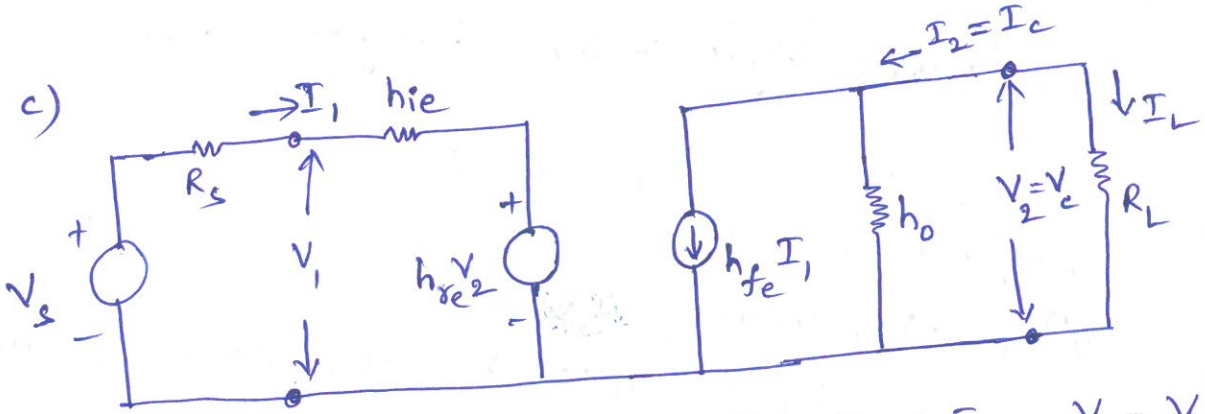
Negative clamper (1M)



b) (2M)



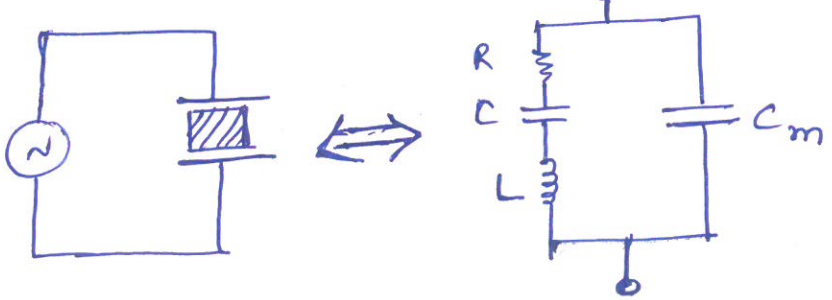
c) (2M)



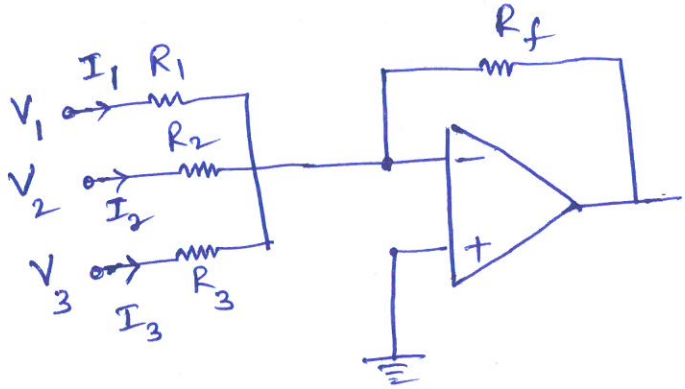
where $V_1 = V_b$, $I_1 = I_b$, $I_2 = I_c$, $V_2 = V_c$ for CE

d) Improves gain by bypassing the emitter resistor through negative feedback (2M)

e) (2M)



f) (2M)



$V_0 = -(V_1 + V_2 + V_3)$

if $R_1 = R_2 = R_3 = R_f = R$.

g) (1M)

Slew rate $= 2\pi f V_p$

for MA 741 op-amp, Slew rate $= 0.5\ V/\mu s$

$0.5 \times 10^6 = 2\pi f \times 1$ (1M)

$\Rightarrow f = 79.6\ KHz$

h) The level translator shifts the DC level so that output becomes 0V when input is 0V and signal is properly centered for symmetrical swing. (2M)

i) Oscillator, pulse generator, ramp & Square wave generator, Traffic light control, burglar alarm (2M)

j) given DAC resolution $= 20mV = 0.02\ V$ (1M)

no. of bits $n = 7$

$V_{FS} = (2^n - 1) \times$ Resolution $= 2.54\ V$

Convert given digital input 1101110 to decimal number $= 110$

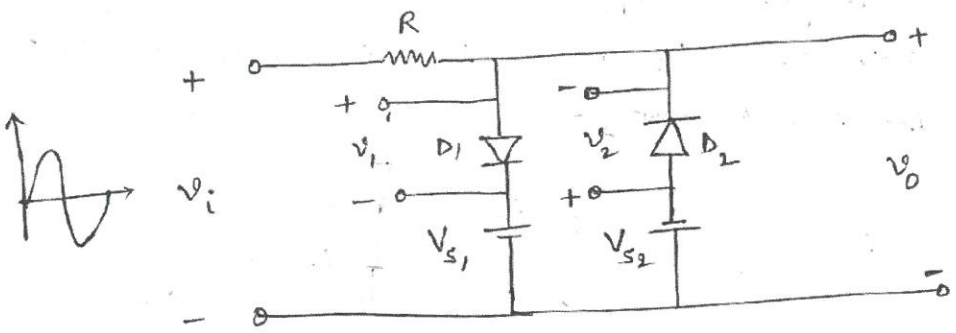
$\therefore V_0 =$ Decimal value $\times$ Resolution (1M)

$= 110 \times 0.02 = 2.2\ V$

Part-B

Unit-I

2.a.



(2M)

First assume that no current is flowing through circuit. Let v_1 and v_2 are the voltages across two diodes D_1 and D_2 with their polarity as shown in the above circuit

The ON & OFF conditions of two diodes can be represented as

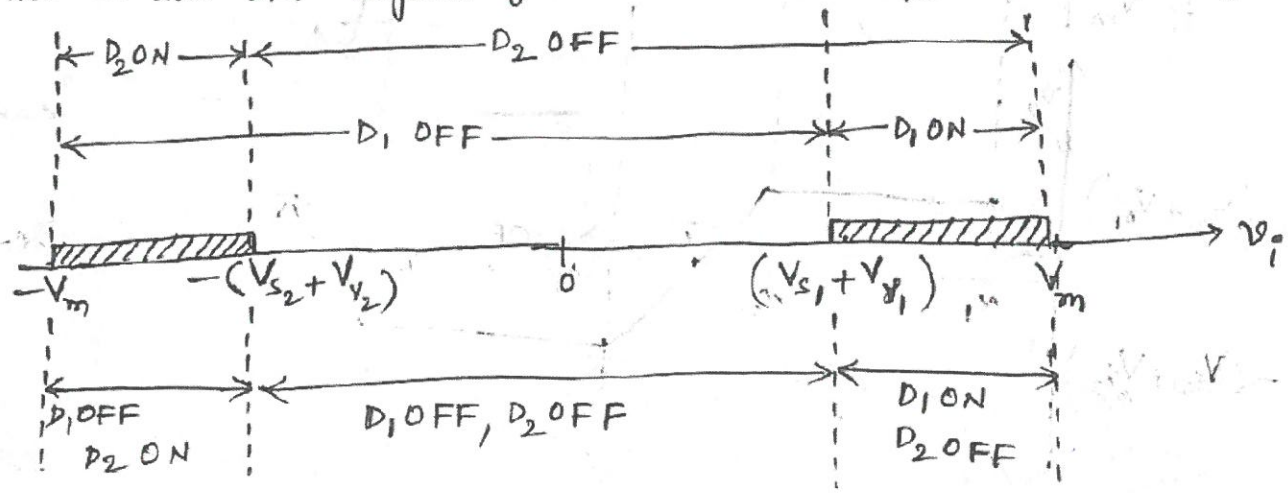
$$\begin{cases} v_i > V_{s_1} + V_{\gamma_1} ; & D_1 \text{ ON} \\ v_i < V_{s_1} + V_{\gamma_1} ; & D_1 \text{ OFF} \end{cases}$$

and

$$\begin{cases} v_i < -(V_{s_2} + V_{\gamma_2}) ; & D_2 \text{ ON} \\ v_i > -(V_{s_2} + V_{\gamma_2}) ; & D_2 \text{ OFF} \end{cases}$$

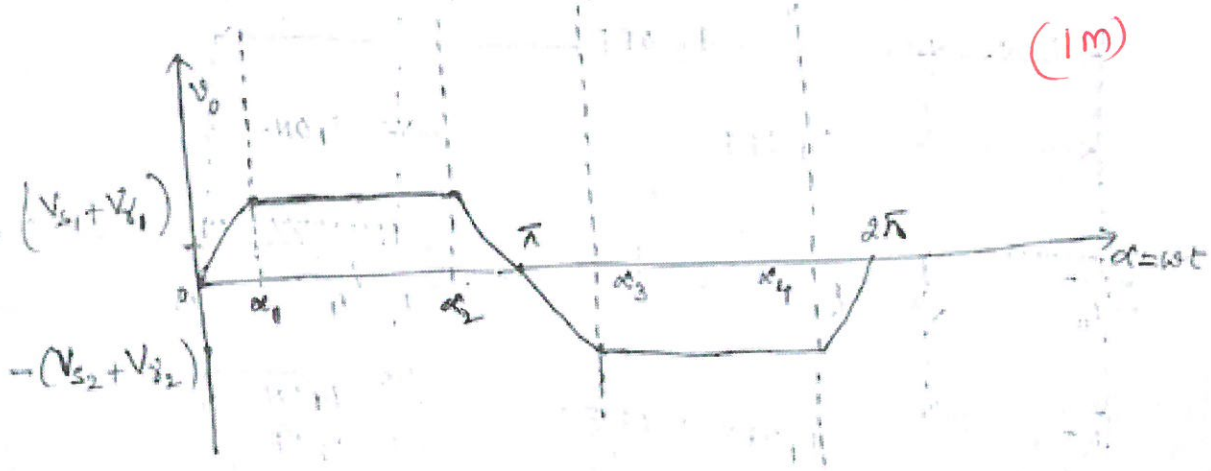
(1M)

The ON and OFF regions of two Diodes D_1 & D_2 are shown as



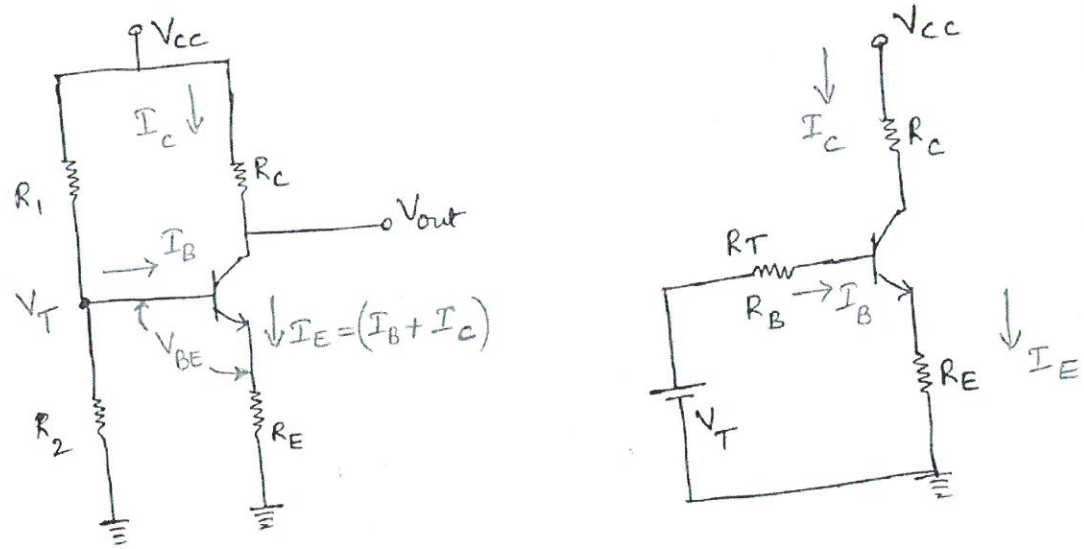
Input	Conducting states of D_1 and D_2	output (1m)
$v_i < -(V_{s_2} + V_{\gamma_2})$	D_1 OFF and D_2 ON	$v_o = -(V_{s_2} + V_{\gamma_2})$
$-(V_{s_2} + V_{\gamma_2}) < v_i < (V_{s_1} + V_{\gamma_1})$	D_1 OFF, D_2 OFF	$v_o = v_i$
$v_i > (V_{s_1} + V_{\gamma_1})$	D_1 ON and D_2 OFF	$v_o = V_{s_1} + V_{\gamma_1}$

(1m)



b)

(3m)



b).

where V_T = Thevenin's Voltage = Voltage drop across R_2

R_T = Thevenins resistance = $R_1 \| R_2$

To find Stability factor (S) (2M)

The loop equation around the base circuit as

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

differentiate with respect to I_C, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)} = \frac{(1+\beta)}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

$$S = (1+\beta)\ \frac{1+\frac{R_B}{R_E}}{1+\beta+R_B/R_E}$$

If R_B/R_E is very small then $S \simeq 1$.

To improve the stability, R_B must be decreased and forcing more current in the voltage devider network of R_1 and R_2

3a)

3.a)

$$\beta = \frac{\alpha}{1-\alpha} = 39 \quad \text{, for Ge Transistor } V_{BE} = 0.3V$$

(i) $$V_T = \frac{R_2}{R_1+R_2} \times V_{cc} = 14.4\ V$$

$$R_T = \frac{R_1 R_2}{R_1+R_2} = 9\ K\Omega$$ (2M)

Loop equation around the base circuit $V_T = I_B R_B + V_{BE} + (I_B + R_c) R_E$

$\Rightarrow$ But $I_B = I_c/\beta$

$\therefore I_c = 6.18\ mA \simeq I_E$ ($\because I_B$ Very Small)

KVL in the output loop $V_{CE} = V_{cc} - I_c R_c - I_E R_E$ (1M)

$\Rightarrow V_{CE} = 14.9\ V$

$\therefore$ Coordinates of Q-point $= (V_{CE}, I_c)$.

$= (14.9\ V, 6.18\ mA)$

ii) Stability factor $S = (1+\beta)\dfrac{1+R_B/R_E}{1+\beta+R_B/R_E}$

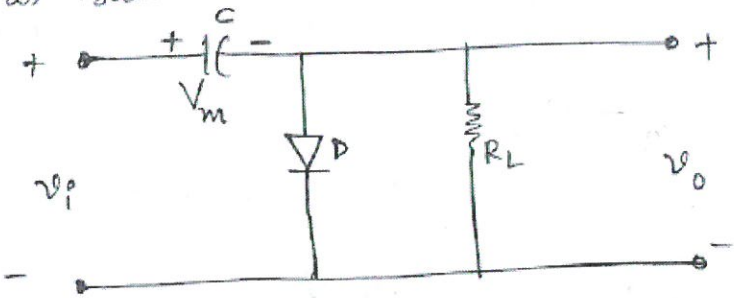
$S = 4.94$ (2M)

b)

b)

Negative clamper

The negative clamper circuit can be obtained by simply reversing the polarities of a diode and capacitor in the positive clamper circuit as shown



(2M)

In this circuit, the diode conducts in the first half of positive cycle and charges the capacitor to the peak voltage V_m with the polarity as shown in the figure. The diode remains in OFF condition in the subsequent cycles and the output is given by.

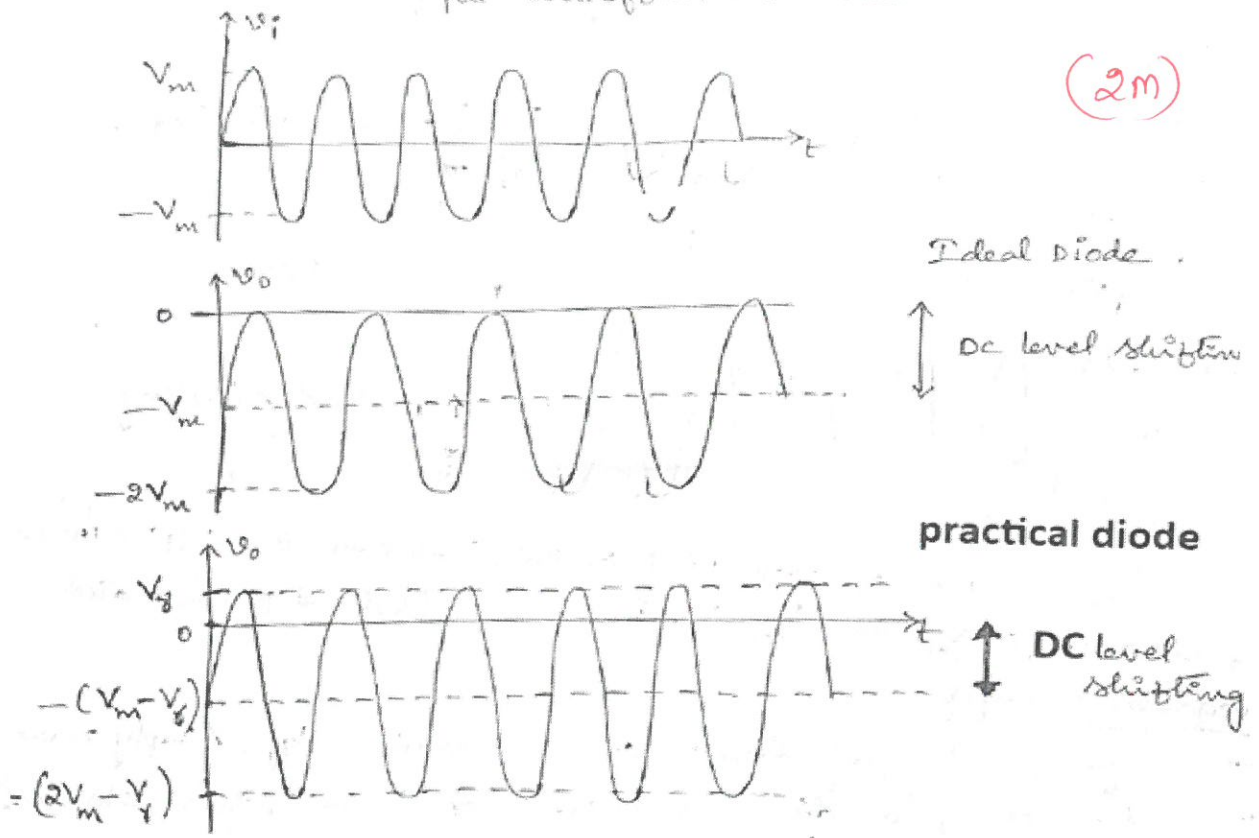
(1M)

$$v_o = -V_m + V_m \sin\omega t$$

for the case of an ideal diode consideration.

For practical diode, the output can be obtained by simply replacing V_m by $-(V_m - V_\gamma)$ in above equation.

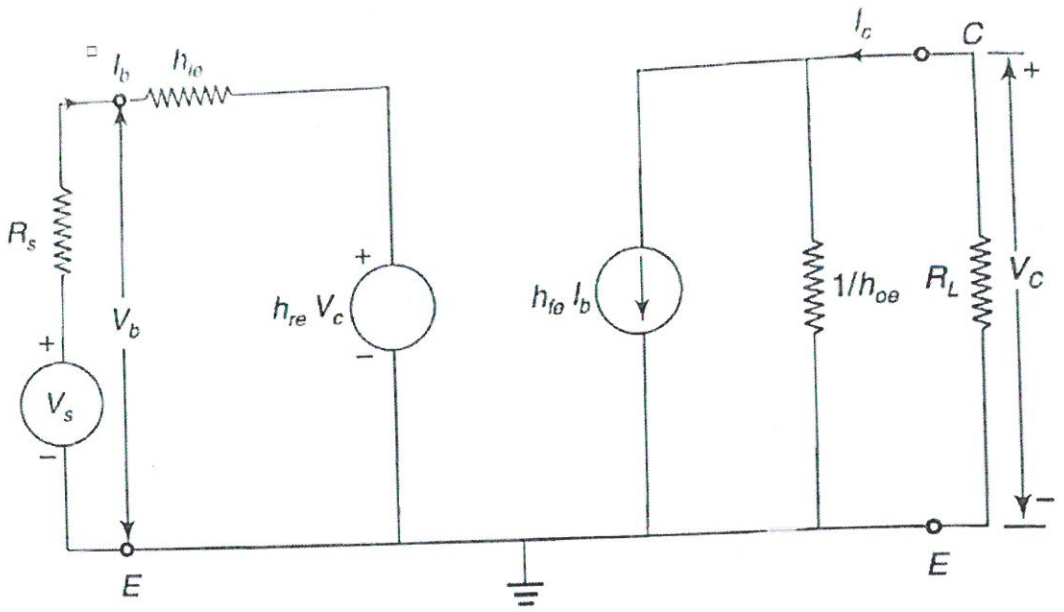
The input and output waveforms are shown below



(2m)

4.a)

4. a)



(2m)

Exact CE hybrid model

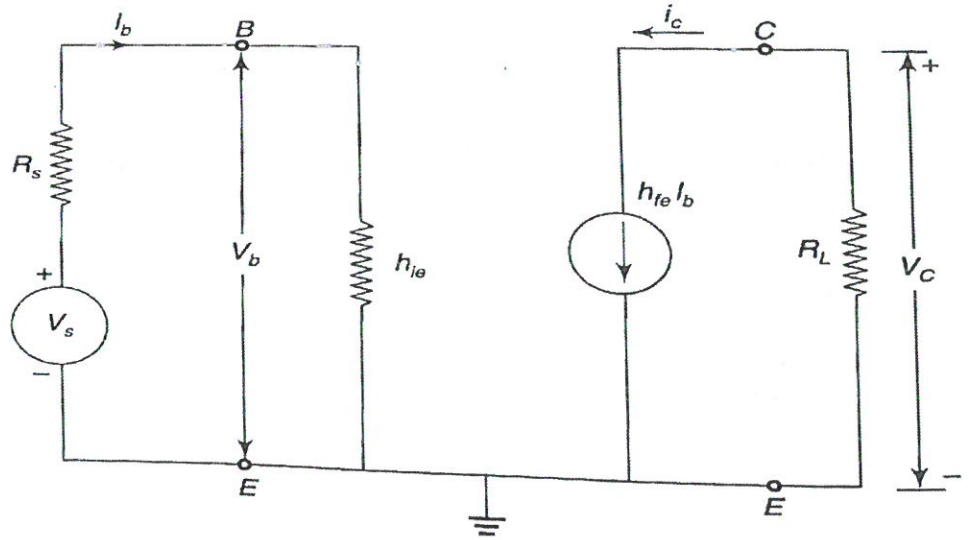
Under this condition, the magnitude of voltage of the generator in the emitter circuit is

$$h_{re}|V_C| = h_{re}I_C R_L = h_{re}h_{fe}I_b R_L$$

(1M)

Since $h_{re}h_{fe} \approx 0.01$, this voltage may be neglected in comparison with the voltage drop across $h_{ie} = h_{it}$ provided that R_L is not too large.

To conclude, if the load resistance R_L is small, it is possible to neglect the parameter h_{re} and h_{oe} and obta the approximate equivalent circuit as shown in Fig. . It can be shown that if $h_{oe}\,R_L \leq 0.1$, the error calculating A_I, A_V, R_i, and R_o for CE configuration is less than 10%.



10/32

Fig. Approximate CE hybrid model

(2m)

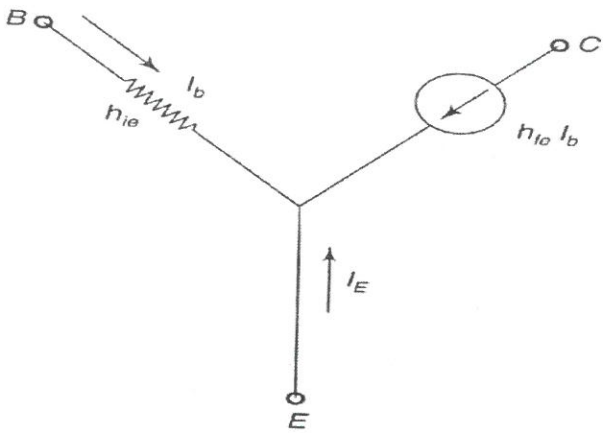


Fig. *Approximate hybrid model valid for all configurations*

b) Given $h_{ie} = 2000\,\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 80$, $h_{oe} = 25\times10^{-6}$ V

$R_L = R_S = 1k\Omega$

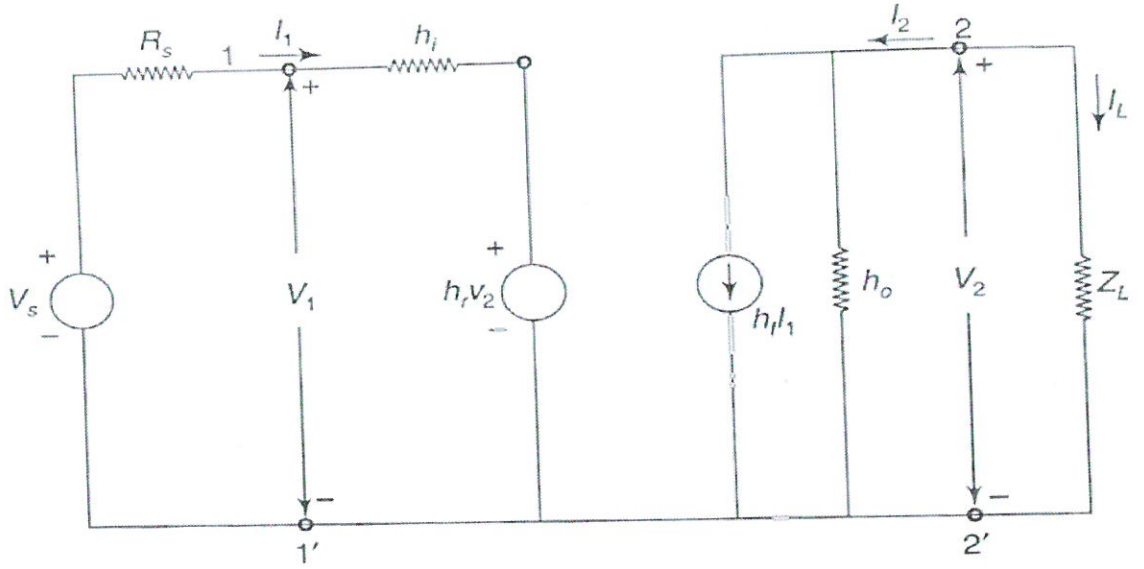
(i) Current gain $A_I = \dfrac{h_{fe}}{1+h_{oe}R_L} = \dfrac{80}{(1+25\times10^{-6}\times1\times10^{3})}$

$A_I = 78.04$ (2m)

(ii) $Z_{in} = h_{ie} - \dfrac{h_{re}h_{fe}}{h_{oe}+1/R_L} = 1984.4\,\Omega$ (1M)

Voltage gain $A_V = \dfrac{-h_{fe}}{\left(h_{oe}+\frac{1}{R_L}\right)Z_{in}} = -39.33$ (2m)

5.a) The exact h-parameter model of a BJT CE amplifier is shown



(2m)

Current Gain or Current Amplification, A_I

For a transistor amplifier, the current gain A_I is defined as the ratio of output current to input current, i.e.,

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

From the circuit of Fig. ,

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$,

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1$$

$$I_2(1 + Z_L h_o) = h_f I_1$$

$$A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}$$

Therefore,

$$A_I = \frac{-h_f}{1 + h_o Z_L}$$

Input Impedance :

$$Z_i = \frac{V_1}{I_1}$$

From the input circuit of Fig. $V_1 = h_i I_1 + h_r V_2$

Hence,
$$Z_i = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$= h_i + h_r \frac{V_2}{I_1}$$

Substituting

$$V_2 = -I_2 Z_L = A_I I_1 Z_L$$

$$Z_i = h_i + h_r \frac{A_I I_1 Z_L}{I_1}$$

(4m)

resulting in

$$Z_i = h_i + h_r A_I Z_L$$

Substituting for A_I,

$$Z_i = h_i - \frac{h_f}{1 + h_o Z_L} h_r Z_L$$

$$= h_i - \frac{h_f h_r}{Z_L \left(\frac{1}{Z_L} + h_o \right)} Z_L$$

Taking the load admittance as $Y_L = \frac{1}{Z_L}$

$$Z_i = h_i - \frac{h_f h_r}{Y_L + h_o}$$

Voltage Gain or Voltage Amplification Factor, A_V

The ratio of output voltage V_2 to input voltage V_1 gives the voltage gain of the transistor, i.e.,

$$A_V = \frac{V_2}{V_1}$$

Substituting $$V_2 = -I_2 Z_L = A_I I_1 Z_L$$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

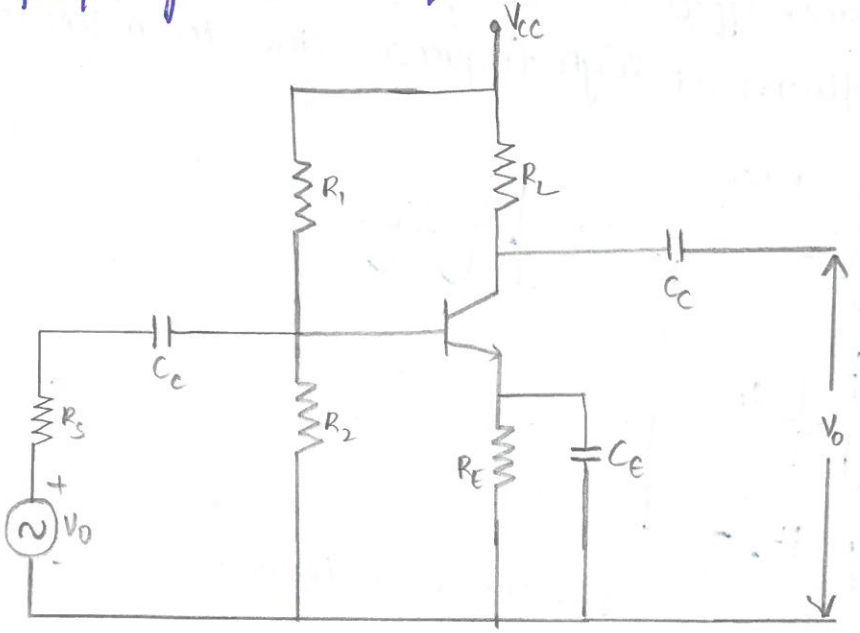
5. Explain the low frequency response of common emitter amplifier. Describing b) the effect of Coupling cacitors, bypass capacitors & internal transistor capacites

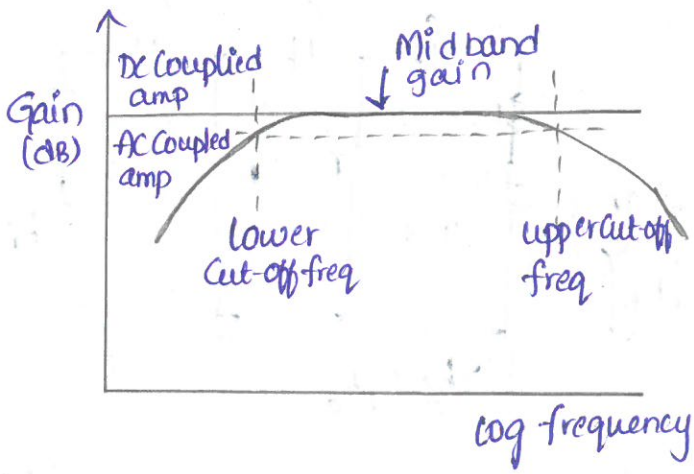
Ans: At low frequencies, the gain of an amplifier decreases due to capacitive reactance X_c of various capacitors present in the circuit. The dominant factors include:

- Coupling capacitors (C_c) - Block dc while allowing AC signals to pass
- Bypass capacitors (C_E) - Improves gain by bypassing the emitter resistor
- Internal transistor capacitances (C_π & C_μ) - Play a significant role at higher frequencies but have negligible effect at very low frequencies

low frequency response of CE Amplifier.

(2M)





Effect of capacitors in CE's Amplifier's low frequency Response

1. Coupling Capacitor
   - → Forms a high-pass filter with Input Impedance.
   - → Cut off frequency is given by: (2m)

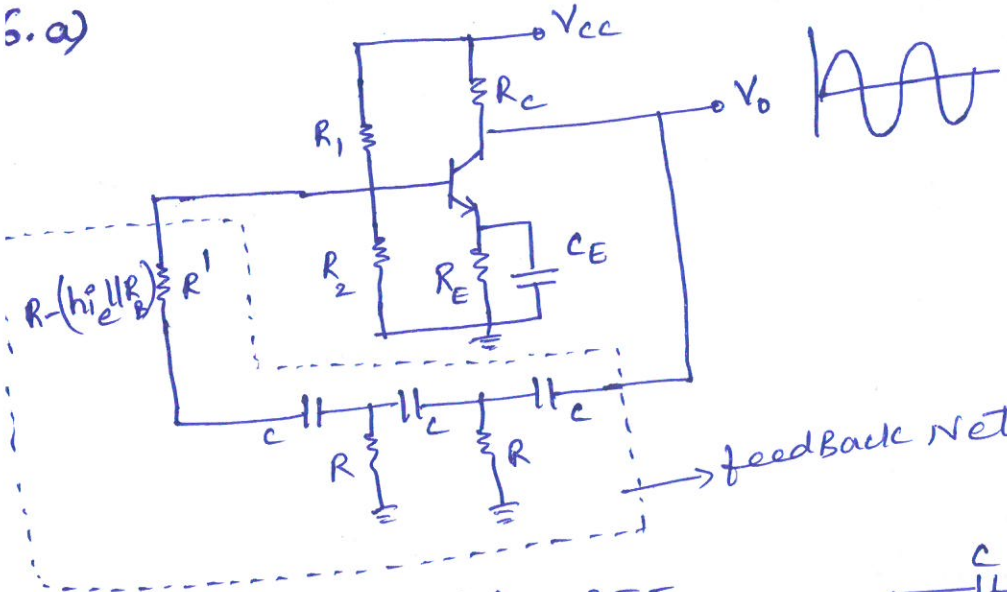
$$f_L = \frac{1}{2\pi R_{in} C_C}$$

2. Bypass Capacitor
   - → Affects the amplifier gain by controlling negative feedback
   - → Cut off frequency due to C_E is:

$$f_E = \frac{1}{2\pi R_E C_E}$$

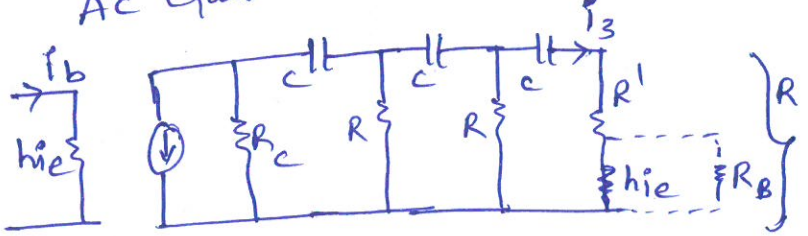
3. Internal capacitances (C_π, C_μ)
   - → have a minor effect at low frequencies
   - → Major influence at high frequencies due to miller effect

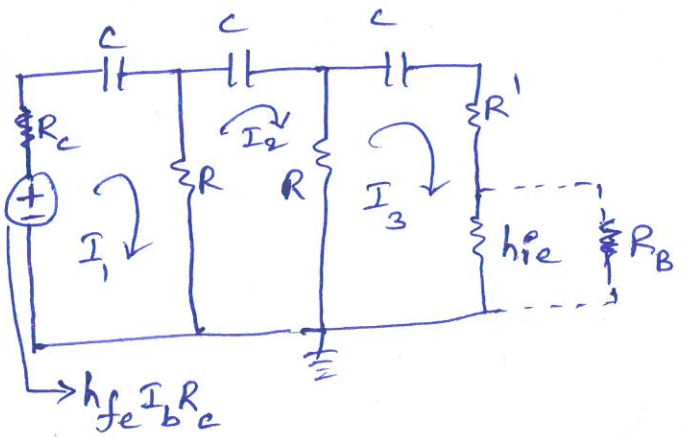
5. a)



(3m)

Ac equivalent model of BJT





$$R = R' + (h_{ie} \| R_B)$$

Above four loops reduced to three loops as

Apply KVL, loop equations are (In frequency domain)

$$\left(2RC+\frac{1}{SC}\right)I_2 - I_1R - I_3R = 0 \longrightarrow (1)$$

$$I_1\left(R_c+\frac{1}{SC}+R\right) - RI_2 = -h_{fe}\,i_b R_c \longrightarrow (2)$$

$$-RI_2 + \frac{1}{SC}I_3 + I_3\left[R+R'+(h_{ie}\,||\,R_b)\right] = 0 \longrightarrow (3)$$

Let $\alpha = \frac{1}{\omega RC}$ and $K = \frac{R_c}{R} \longrightarrow (4)$

Put $S = j\omega$ in above equations and put eq (4) in equations (1), (2), (3)

Then $I_2 = I_3(2-j\alpha) \longrightarrow (5)$ (3m)

$$I_1 = I_3(3-\alpha^2-j4\alpha) \longrightarrow (6)$$

put (5) & (6) in equation (2)

Then $$I_3/I_b = \frac{-h_{fe}\,K}{1+3K-(5+K)\alpha^2 - j\left[(6+4K)\alpha-\alpha^3\right]}$$

$\longrightarrow (7)$

for sustained oscillations,

at $\omega = \omega_0$, the gain is real.

where ω_0 = Frequency of oscillation in rad/sec.

f_0 = Frequency of oscillation in Hz.

In eq (7), equate imaginary part to zero.

$$(6+4K)\alpha - \alpha^3 = 0$$

$$\alpha\left[(6+4K)-\alpha^2\right] = 0 \Rightarrow \alpha^2 = 6+4K \quad (\because \alpha \neq 0)$$

$$\left(\frac{1}{\omega_0 RC}\right)^2 = 6+4K$$

$$\Rightarrow \omega_0 = \frac{1}{RC\sqrt{6+4K}}$$

$$\Rightarrow f_0 = \frac{1}{2\pi RC\sqrt{6+4K}}$$ called frequency of oscillation

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from magnitude criteria $|A\beta| = 1$

$$1 = \frac{-h_{fe} K}{(1+3K) - (5+K)\alpha^2} \quad \left(\because (6+4K)\alpha - \alpha^3 = 0 \text{ in eq (7)}\right)$$

then $h_{fe} \geq 4K + 23 + \frac{29}{K}$ where $K = \frac{R_c}{R}$

To find minimum value of h_{fe}.

$$\frac{d h_{fe}}{dK} = 4 + 0 - \frac{29}{K^2} = 0 \Rightarrow K = 2.7$$

Then $h_{fe} \geq 44.5$.

)

open loop gain $A_{OL} = \infty$

Input impedance $R_i = \infty$

output impedance $R_0 = 0$

Bandwidth, $BW = \infty$ (2m)

Zero offset ie, $V_0 = 0$ when $V_1 = V_2 = 0$

i) Op-amp draws no current from input terminals ($I_1 = \frac{I}{2} = 0$)

Because of infinite input impedance, any signal source can drive it and there is no loading on preceding driver stage

ii) Since gain is ∞, the voltage between inverting and Non inverting terminals ie, differential input voltage $V_d = V_1 - V_2$ is essentially zero for finite output voltage V_0. (2M)

iii) V_0 is independent of the current drawn from the output as $R_0 = 0$. The output has can drive an infinite no. of other devices.

A practical op-amp is not an ideal op-amp which has $A_{OL} \neq \infty$, $R_i \neq \infty$, $R_0 \neq 0$.

7. a) Slew rate (3M)

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs.

for example, 1 V/μs slew rate means that the output rises or falls by 1V in one micro second.

practical IC op-amp's have specified slew rates from 0.1 V/μs to well above 1000 V/μs.

for μA741 op-amp, Slew rate = 0.5 V/μs

$$\therefore \quad SR = \left.\frac{dV_o}{dt}\right|_{max} = 2\pi f V_p$$ where V_p = peak voltage

7. b) Crystal oscillator: The use of piezo electric crystals in parallel resonant circuits provide high frequency stability in oscillators. Such oscillators are called as Crystal Oscillators. The principle of Crystal oscillators depends on piezo electric eff (1M)

Working of a Quartz Crystal

Inorder to make a crystal work in an electronic circuit the crystal is placed between two metal plates in the form of a capacitor and the ac voltage is aplied in parallel to the crystal as (1M)

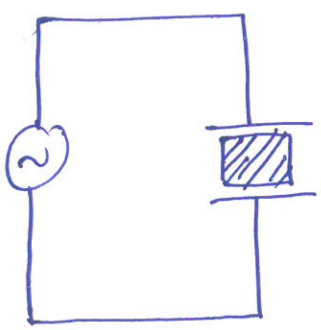
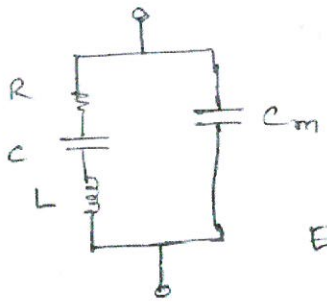


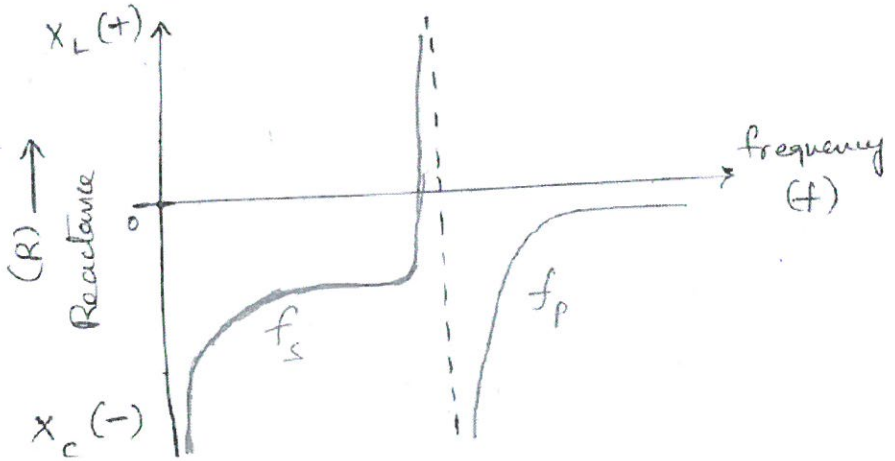
fig - Symbol of a Crystal



(1m)

Equivalent circuit of a Crystal

The frequency response of a crystal is shown below



(2m)

here, the crystal has two closely spaced resonant frequencies
- Series resonant frequency (f_s)
- parallel " " (f_p)

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$f_p = \frac{1}{2\pi\sqrt{LC_T}} \quad \text{where } C_T = \left(\frac{C C_m}{C + C_m}\right)$$

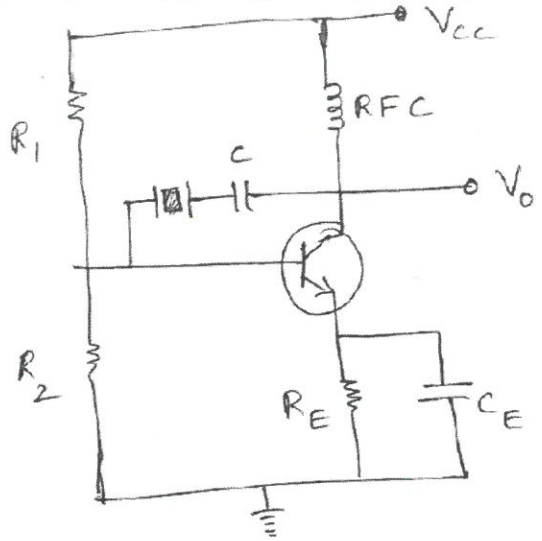
Value of C_m is usually very large as compared to C.

Therefore value of $C_T \simeq C$.

Hence $f_s \simeq f_p$.

Crystal oscillator circuit

(2m)



The crystal is connected as a series element in feed back path from collector to base. The resistor R_1 R_2 and R_E provide a voltage divider stabilized dc bias circuit.

Capacitor C_E provides a ac bypass of the emitter resistor and RFC (radio frequency choke) coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal.

The circuit frequency of oscillation is set by the series resonant frequency of a crystal and its value is given by

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

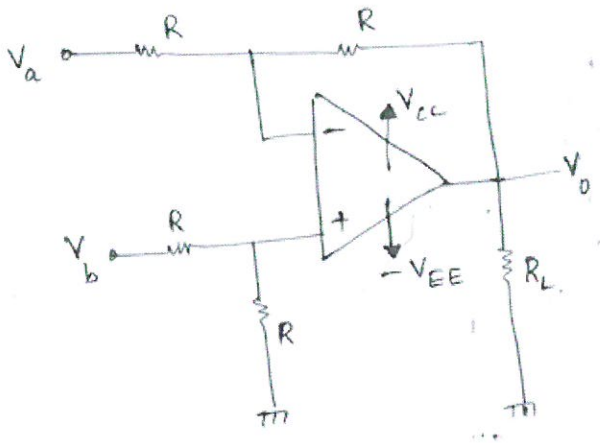
The advantages of a crystal oscillator are

* They have a high orders of frequency of stability
* The Quality factor (Q) of a crystal is very high.

The disadvantages of crystal oscillator are

* They are easily damaged and broken do can be used in low power circuits
* The frequency of a oscillations cannot be changed more

8.a)



(2m)

In this circuit, all external resistors are equal in value. So the gain of amplifier is equal to 1.

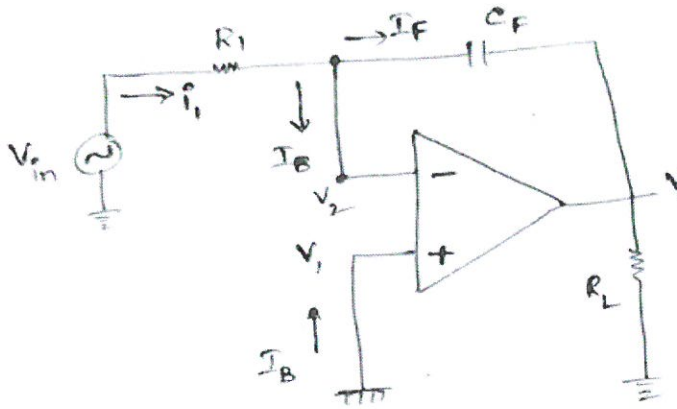
The output voltage of a differential amplifier with a gain of 1 is $V_0 = -\frac{R}{R}(V_a - V_b)$ (2m)

$$\Rightarrow V_0 = V_b - V_a$$

b)

Integrator

A circuit in which the output voltage waveform is the integral of input voltage waveform is the integrator (or) the integrating amplifier is shown (3m)



$$V_0 = -\frac{1}{R_1 C_F}\int_0^t V_{in}\,dt + c$$

Apply KCL at node v_2

$$i_1 = i_B + i_F$$

$$\Rightarrow \quad i_1 \simeq I_F \quad (\text{since } i_B \text{ is negligibly small})$$

$$\frac{V_{in} - V_2}{R_1} = C_F \frac{d}{dt}(v_2 - v_0)$$

Since $v_1 = v_2 = 0$ Then integrate with respect to time on both sides

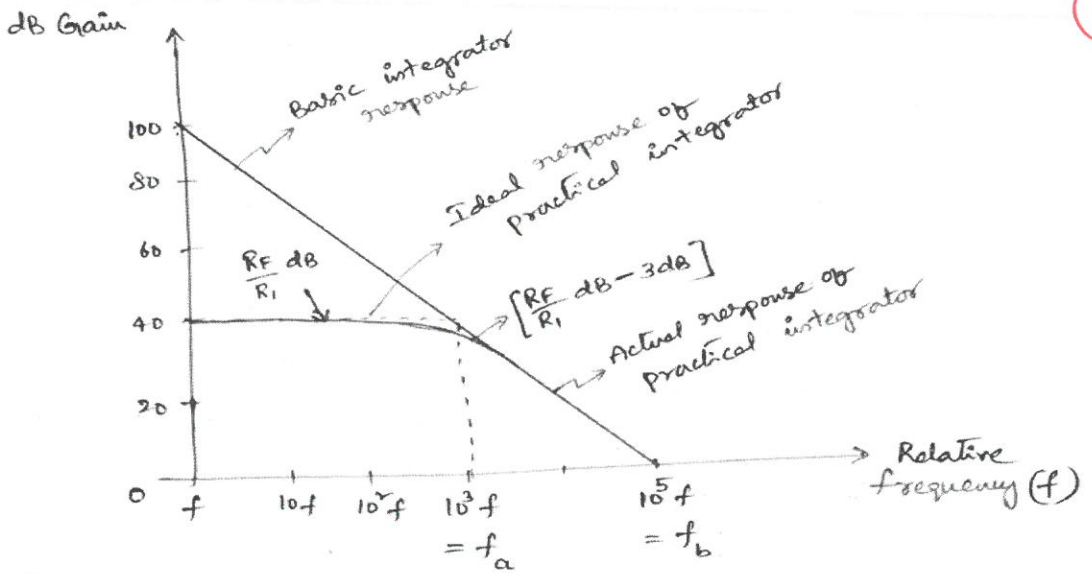
$$\int_0^t \frac{V_{in}}{R_1}\, dt = \int_0^t C_F \frac{d}{dt}(-v_0)\, dt$$

$$= C_F(-v_0) + v_0\Big|_{t=0}$$

$$\therefore \quad v_0 = -\frac{1}{R_1 C_F}\int_0^t v_{in}\, dt + c \qquad (1m)$$

where c is integration constant and is proportional to v_0 at $t = 0$.

(2m)



In above graph, f_b is the frequency at which the gain is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

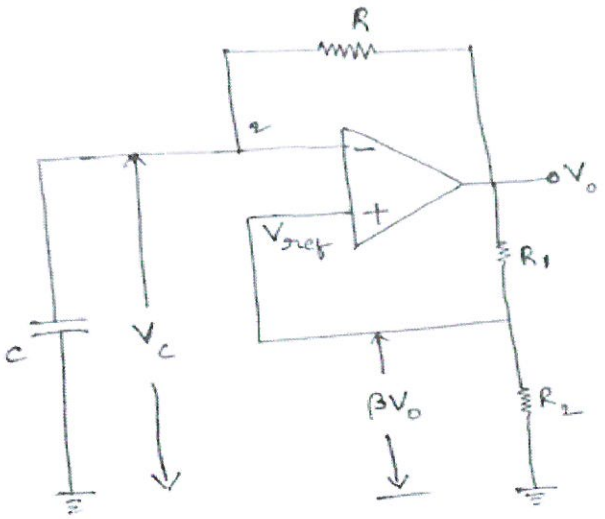
In between f_a to f_b, the circuit acts as an integrator. The gain limiting frequency f_a is $f_a = \frac{1}{2\pi R_F C_F}$; In general f_a, $R_1 C_F$ & $R_F C_F$ selected such that $f_a < f_b$

9.a)

Square wave Generator

Also called Astable Multivibrator, free running oscillator. The principle of operation of square wave output is to force an op-amp to operate in the saturation region.

Simple op-amp square wave generator is shown (2M)

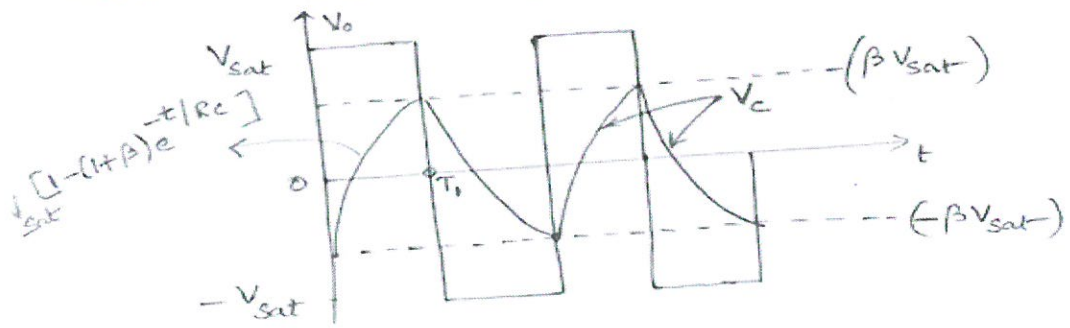


A fraction of output $\beta = \left(\frac{R_2}{R_1 + R_2}\right)$ is fed back to the (+) input.

Thus the reference voltage $V_{ref} = \beta V_o$ and may take values $+\beta V_{sat}$ (or) $-\beta V_{sat}$

When $V_i > V_{ref}$ then switching takes place resulting in a square wave output.

When $V_o = +V_{sat}$, the capacitor now starts charging towards $+V_{sat}$ through R as shown (2M)



The voltage at (+) input terminal is held at $+\beta V_{sat}$ by R_1 and R_2. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat} = V_{ref}$.

When the voltage at (−) input terminal $> V_{ref} = \beta V_{sat}$ then the output is goes to $-V_{sat}$. At this time, $V_c = +\beta V_{sat}$.

It begans to discharge through R, that is charges towards $-V_{sat}$. When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats itself as shown in above waveforms.

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa.

The voltage across capacitor as a function of time t is

$$v_c(t) = V_f + (v_i - V_f)\, e^{-t/RC} \qquad (1M)$$

where $V_f = +V_{sat}$ (final voltage)

$v_i = -\beta V_{sat}$ (Initial ")

$$\therefore \quad v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

(or) $$v_c(t) = V_{sat} - V_{sat}(1+\beta)\, e^{-t/RC}$$

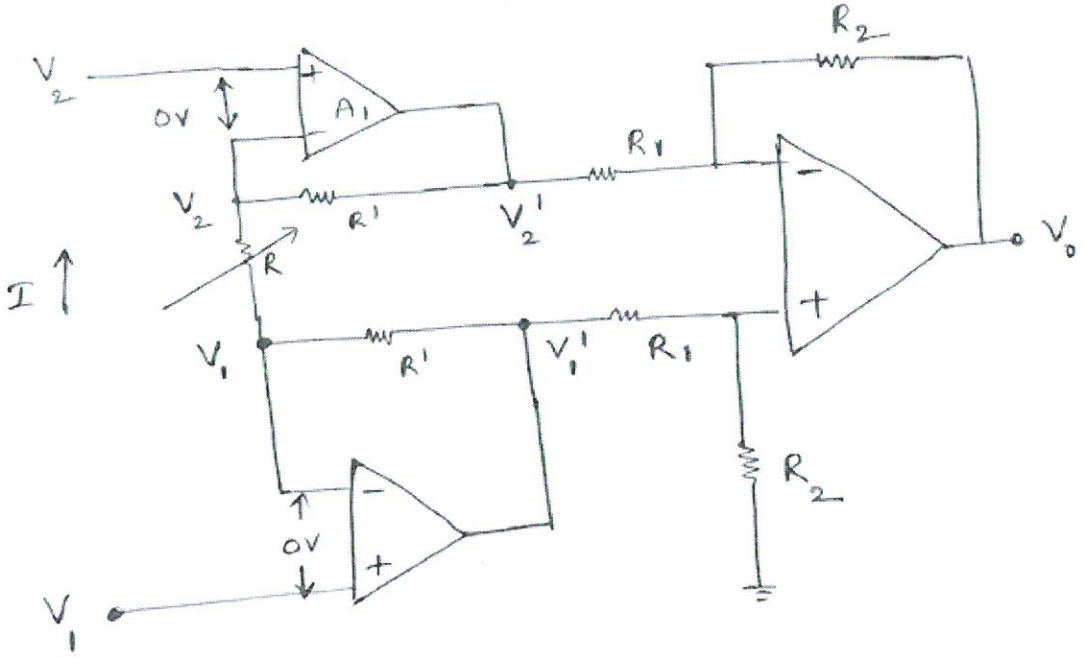
At $t = T_1 \Rightarrow v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)\, e^{-T_1/RC}$

After algebric manipulation, $T_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right)$ for half period

Total period $T = 2T_1 = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$

and the output waveform is Symmetrical.

b) (2M)



The op-amps A_1 and A_2 have differential input voltages as as zero. For $V_1 = V_2$, that is under Comman mode condition, the voltage across R will be zero. As no current flows through R and R' the non-inverting amplifies A_1 acts as voltage follower, so its output $V_2' = V_2$. (1M)

Similarly op-amp A_2 acts as voltage follower having output $V_1' = V_1$. However, if $V_1 \neq V_2$, current flows in R and R' and $(V_2' - V_1') > (V_2 - V_1)$.

Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit.

Using super position theorem,

$$V_0 = -\frac{R_2}{R_1} V_2' + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1 + R_2}\right) \qquad (2M)$$

$$V_0 = \frac{R_2}{R_1}\left(V_1' - V_2'\right) \longrightarrow (1)$$

Since no current flows into op-amp, the current I flowing (upwards) in R is $I = (V_1 - V_2)/R$ and passes through R'.

$$V_1' = R'I + V_1 = \frac{R'}{R}(V_1 - V_2) + V_1$$

and $$V_2' = -R'I + V_2 = -\frac{R'}{R}(V_1 - V_2) + V_2$$

from eq (1)

$$V_0 = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

$$\Rightarrow V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2).$$

The difference gain of this instrumentation amplifier can be varied by replacing the resistance R by a potentiometer in above second circuit.

10.a)

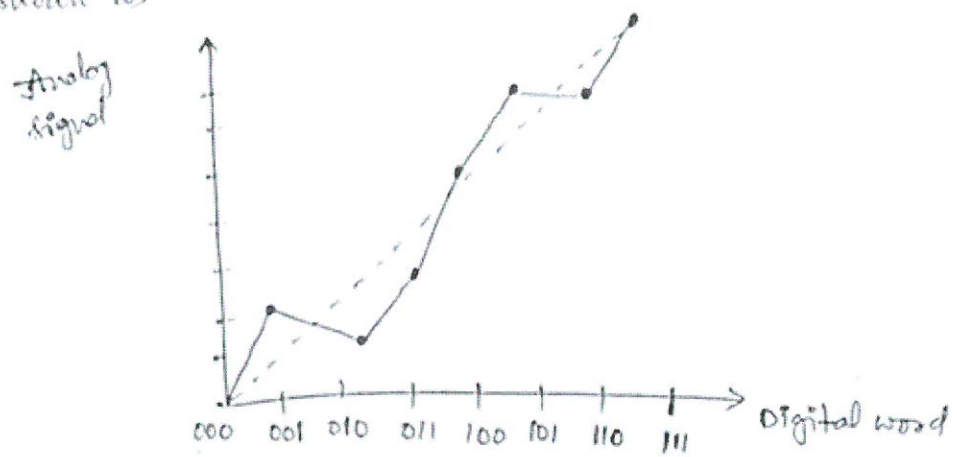
(1M)

Resolution :- It is the smallest change in voltage which may be produced at the output (of input) of a converter. For example, an 8-bit D/A converter has $2^8 - 1 = 255$ equal intervals. Hence the smallest change in output voltage is $\frac{1}{255}$ of the full scale output range. In short, the resolution is the value of LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment}$$

Monotonicity :- whose analog output increases for an increase in digital input. The transfer curve for a non-monotonic DAC is shown as

(1M)



Since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications otherwise oscillations can produce.

(1 M)

Settling Time :- The time taken for the output to settle within a specified band $\pm \frac{1}{2}$ LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Conversion time : (1 M)

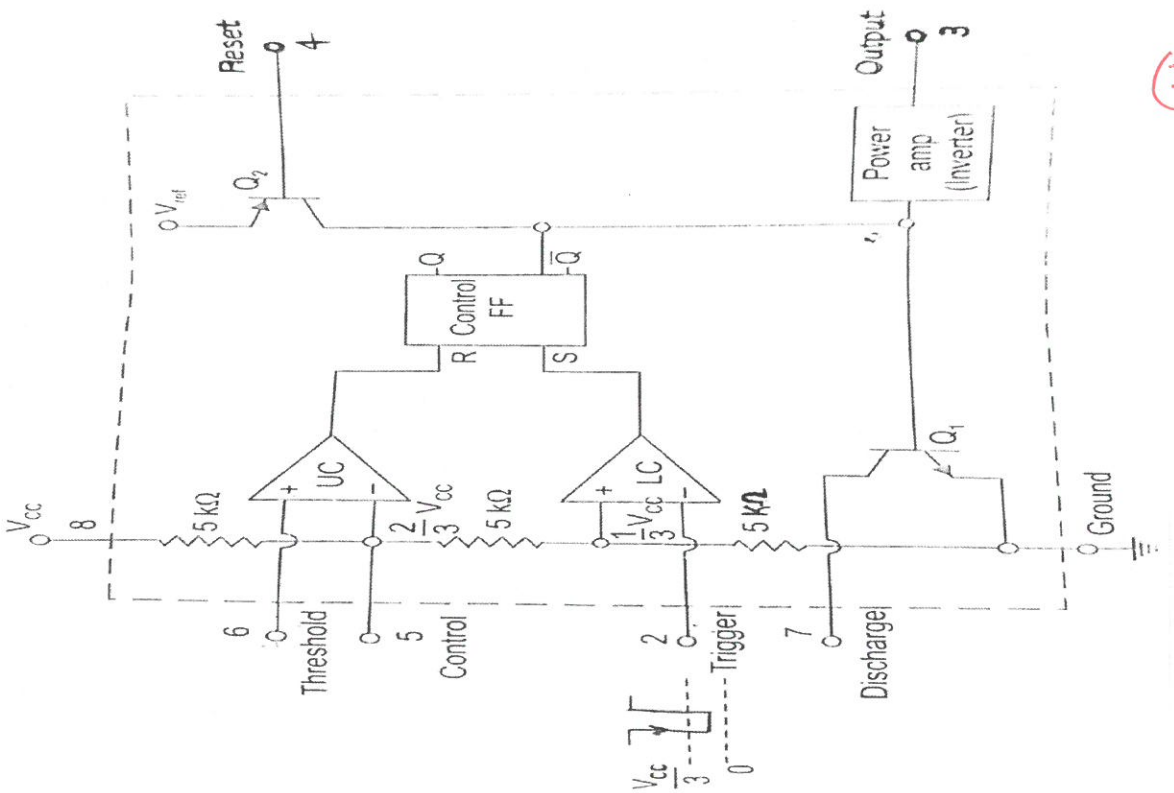
The conversion time is the total time taken by a converter (ADC or DAC) to convert a signal from one form to another:

- In an Analog-to-Digital Converter (ADC):
  Time taken to convert an analog signal into a digital output
- In a Digital-to-Analog Converter (DAC):
  Time taken to convert a digital input into an analog signal

b)

Description of Functional Diagram

(3 M)



Three 5K resistors are present internally. These resistors act as voltage devider, providing bias voltage of $\frac{2}{3} V_{cc}$ to upper comparator (UC) and $\frac{1}{3} V_{cc}$ to lower comparator (LC).

where V_{cc} is supply voltage. (3M)

Since these two voltages fix the necessary comparator threshold voltages,

They are used to determine the timing interval. It is possible to vary time electronically also by applying a modulation voltage to the control voltage input terminal (pin 5).

In the standby (stable) state, the output Q of the control flip flop (FF) is high. This makes the output LOW because of power amplifier which is basically an inverter.
A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of lower comparator $\left(\frac{V_{cc}}{3}\right)$. At the negative going edge of trigger, as the trigger passes through $\left(\frac{V_{cc}}{3}\right)$, the output of lower comparator goes HIGH and sets the FF $(Q=1, \bar{Q}=0)$.
During the positive excursion, when the threshold voltage at pin 6 passes through $\frac{2}{3} V_{cc}$, the output of UC goes high. and resets the FF $(Q=0, \bar{Q}=1)$.

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The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4V. When this reset is not used, it is returned to V_{cc}. The Transistor Q_2 serves as a buffer to isolate the reset input from the FF and Transistor Q. The Transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

→ 11.a) The Voltage Controlled Oscillator (VCO) is a key building block in a Phase-Locked Loop (PLL), and its main function is to generate an output signal whose frequency is controlled by an input voltage (1M)

Applications of VCO (IC 566)

A VCO (566) can be used in various applications, including function generation, tone generation, FM modulation, frequency shift keying (FSK), and as a clock generator,

1. Function Generator: (3M)

VCOs can generate various waveforms (sine, square, triangle) by varying the control voltage, making them useful for creating test signals or audio tones.

2. Tone Generator:

By controlling the VCO's frequency with a voltage, you can create tones or musical notes, useful in audio applications or musical instruments.

3. FM Modulation:

VCOs are a key component in FM modulation, where the frequency of the carrier signal is varied in accordance with the modulating signal.

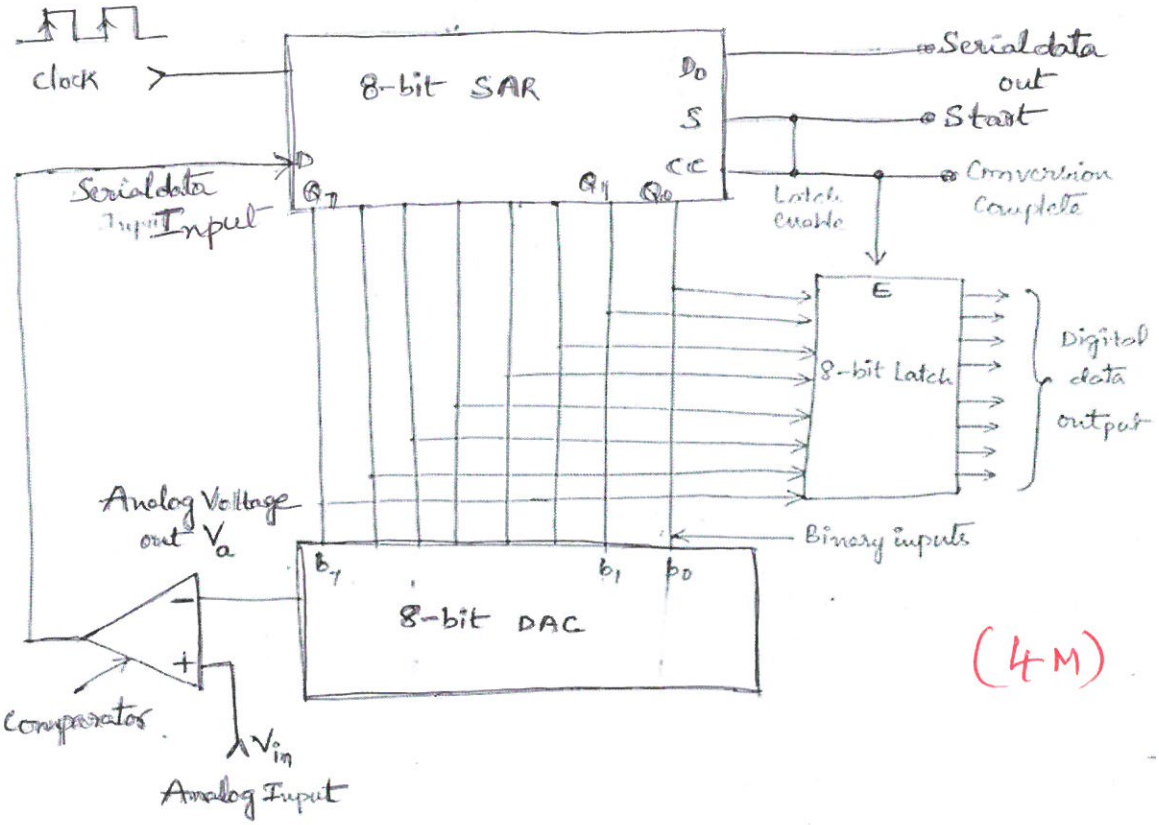
4. Frequency Shift Keying (FSK):

VCOs can be used to generate different frequencies for FSK, a modulation technique where data is transmitted by changing the frequency of a carrier signal.

5. Clock Generator:

VCOs can provide a stable and adjustable clock signal, which is essential for synchronizing digital circuits and systems.

b)



(4M)

The analog output V_a of DAC is then ~~applied to one 8 bit~~ (2M) compared to an analog input signal V_{in} by the comparator. The output of a comparator is a serial data input to the SAR. The SAR then adjusts its digital output (8 bits) until it is equivalent to analog input V_{in}. The 8-bit latch at the end of conversion holds onto the resultant digital data output. The circuit works as follows. At the start of a conversion cycle, the SAR is reset by holding the Start (S) signal high. On the first cycle, pulse LOW to HIGH transition, the MSB Q_7 of the SAR is set. The D/A converter then generates an analog equivalent to Q_7, which is compared with the analog input V_{in}. If the comparator output is low, the DAC output $> V_{in}$ and the SAR will clear its MSB Q_7. On the other hand, if comparator output is high, the D/A output $< V_{in}$ and the SAR will keep MSB Q_7 set.

In Next cycle, Q_6 will be tested by SAR to either keep or clear it This process is continued upto last bit Q_0. Then SAR forces CC signal HIGH to indicate the parallel output lines contains valid digital data which is hold by 8-bit latch.

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