PVP 23

Code: 23ES1304

II B.Tech - I Semester – Supplementary Examinations - MAY 2025

DIGITAL LOGIC AND COMPUTER ORGANIZATION

(Common for CSE, IT)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

PART – A

1.a)	Convert the binary number 111101.011011 to hexadecimal number.
b)	State DeMorgan's theorem.
c)	Realize XOR gate using only NAND gates.
d)	What is race around condition? How do you eliminate it?
e)	Compare single address and two address instructions.
f)	Draw the hardware structure for Booth's multiplication.
g)	Distinguish between ROM and RAM memories.
h)	Compare main memory and Auxiliary memory in terms of speed and capacity.
i)	Explain the principle of cache memory.
j)	What is need for an I/O interface?

PART – B

					Max. Marks
UNIT-I					
2	a)	Prove using DeMorgan's theorem that XOR and XNOR gates are complements of each other.			5 M
	b)	Construct the truth table for the following function F= (xy +z) (y + xz).			5 M
OR					
3	a)	Simplify the following function using K-map f(a, b, c, d)= π(0, 1, 2, 4, 7, 8, 9, 10, 13, 14, 15)			5 M
	b)	Define the following: i. Implicant, ii. Prime Implicant, iii. Essential prime Implicant using K-maps with examples.			5 M
UNIT-II					
4	a)	Compare among signed magnitude form, 1's complement and 2's complement representation.			5 M
	b)	Design 4x2 priority encoder with a valid indicator using suitable gates.			5 M
OR					
5	a)	Explain 4-bit universal shift register with a neat block diagram.			5 M
	b)	Design Mod-5 synchronous up counter using JK MS flip-flops and draw logic diagram.			5 M
UNIT-III					
6	a)	Explain memory stack of general purpose computer.			5 M

	b)	Explain any five addressing modes of computer with examples.	5 M
OR			
7	a)	Discuss hardware implementation of signed magnitude for addition and subtraction.	5 M
	b)	Explain principles of decimal addition and subtraction with numerical examples.	5 M
UNIT-IV			
8	a)	What is ROM? Explain types of ROMs with its structures.	5 M
	b)	Discuss important characteristics, merits and demerits of magnetic Disks.	5 M
OR			
9	a)	Explain in detail about Direct mapping cache organization.	5 M
	b)	Explain the method of translating virtual address to physical address.	5 M
UNIT-V			
10	a)	Compare and contrast between memory mapped I/O and I/O mapped I/O in terms of capacity, address bits, decoding, merits and demerits.	5 M
	b)	Explain strobe controlled asynchronous serial data transfer.	5 M
OR			
11	a)	Summarize programmed I/O and Interrupt driven I/O.	5 M
	b)	Explain three modes of DMA operation.	5 M